

Letters

Phase Feedforward Control for Single-Phase Boost-Type SMR

Hung-Chi Chen, *Member, IEEE*, Heng-Yi Li, and Ru-Shiuan Yang

Abstract—In this letter, a phase feedforward control (PFFC) for a single-phase boost-type switching-mode rectifier is addressed. In the conventional input voltage feedforward loop, the feedforward signal is fixed regardless of the load level. The proposed phase feedforward signal adjusts according to the load level without sensing the load current. The simulated and experimental results also demonstrate the effectiveness of proposed PFFC. Compared to a conventional feedforward signal, relatively small proportional gain can be used in the proposed PFFC without loss of current tracking performance, which would also increase the overall system immunity against noise.

Index Terms—AC–DC power conversion.

I. INTRODUCTION

THE USE of switching-mode rectifier (SMR) with power factor correction (PFC) function is an effective mean to perform the qualified ac/dc conversion. In general, the PFC function includes the input current waveform shaping and the output dc voltage regulation.

The boost-type SMRs are the most popular circuit topology among all the others for their continuous current in the front-end inductors [1]. In a boost-type SMR, large-scale input voltage variation can be seen as a disturbance. It follows that input voltage feedforward loops [2]–[6] for boost-type SMRs can be found often in the literature.

The concept of the input voltage feedforward loop is to generate a “nominal duty ratio pattern” from the rectified input voltage. This nominal duty ratio pattern effectively produces an average voltage across the switch equal to the instantaneous rectified input voltage. However, it is noted that this nominal duty ratio pattern is fixed regardless of load condition [3]–[5], i.e., the conventional input feedforward signal at heavy load is the same as that at light load. It implies that the performance of current shaping function would be degraded at heavy load. To overcome it, several load feedforward loops without sensing load current had been proposed in [6], [7] where the load condition is estimated from the reference current. The proposed phase feedforward control (PFFC) can be regarded as a combination of input voltage feedforward control and load feedforward control.

In PFFC, the original phase feedforward signal is also generated from the rectified input voltage and then delayed through

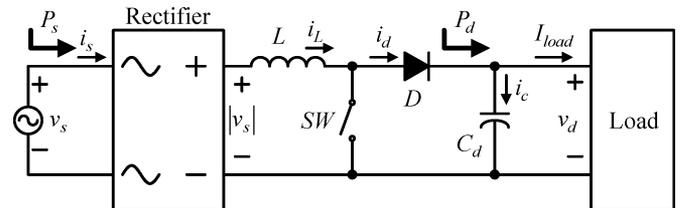


Fig. 1. Power circuit of the boost-type SMR.

phase shifter according to the current reference magnitude. The larger the current magnitude is, the more the shifting phase of phase feedforward signal can be found. Compared to the conventional input voltage feedforward control, the proposed PFFC is able to adjust the feedforward signal according to the load level and relatively small proportional gain can be used to yield the desired current tracking performances and increase the overall system immunity against noise.

From the viewpoint of implementation, the proposed PFFC can also be seen as a combination of a phase shifter with varying phase and two “fixed gain” blocks. It is well-known that implementing a phase shifter with varying phase in analog circuit is significantly harder than that in a digital system [like DSP/field-programmable gate array (FPGA)]. Therefore, there is near-zero complexity added to the digital implementation of PFFC.

After the development of PFFC, we also find that the proposed PFFC can be seen as various implementations of the “full feedforward control,” and therefore, the performance improvement of PFFC is limited compared to [7]. However, implementing “full feedforward control” in analog circuits is easier than that in a digital system due to its calculation load of current loop, such as the PI current controller and derivative of the reference current. Therefore, “full feedforward control” is preferred in an analog circuit and the proposed PFFC is suitable for a digital PFC controller.

II. CONVENTIONAL FEEDFORWARD CONTROL

Power circuit configuration of a boost-type SMR is shown in Fig. 1. The circuit mainly consists of a diode bridge rectifier and a boost-type dc/dc converter. The input voltage v_s can be expressed by $\hat{V}_s \sin(2\pi f_{in} t)$, where f_{in} is the input line frequency. To simplify the analysis, some assumptions are made.

- 1) The circuit components are lossless and the circuit includes a reasonable bulk capacitor C_d .
- 2) The switching frequency f_{tri} is significantly higher than the line frequency f_{in} .

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The authors are with the Department of Electrical and Control Engineering (ECE), National Chiao Tung University (NCTU), Hsinchu 30010, Taiwan (e-mail: hcchen@cn.nctu.edu.tw; hyli@iner.gov.tw; rushiuan@gmail.com).

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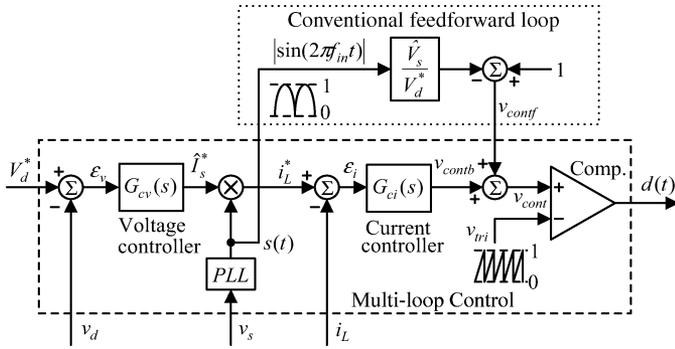


Fig. 2. Multiloop control with conventional feedforward loop.

As shown in Fig. 2, the multiloop control is composed of an inner current controller $G_{ci}(s)$ and an outer voltage controller $G_{cv}(s)$. In order to regulate the output voltage v_d to desired command V_d^* , the reference input current peak \hat{I}_s^* can be tuned by the voltage controller $G_{cv}(s)$. Multiplying \hat{I}_s^* by the rectified sine signal $s(t) = |\sin(2\pi f_{in}t)|$ yields the desired inductor current command i_L^* as the reference current for inner current controller $G_{ci}(s)$. Then, the physical switching signal $d(t)$ for switch SW in Fig. 1 is generated by comparing the control signal v_{cont} and the triangular signal v_{tri} at the comparator's (+) terminal and (-) terminal, respectively.

Because of the assumed bulk capacitor C_d and the use of an outer voltage controller, the output voltage v_d in steady state can be assumed to be equal to the desired dc voltage $v_d = V_d^*$. Thus, according to the state of the switch SW, the inductor voltage can be expressed by

$$v_L = |v_s| = \left| \hat{V}_s \sin(2\pi f_{in}t) \right|, \quad \text{when SW ON} \quad (1)$$

$$v_L = \left| \hat{V}_s \sin(2\pi f_{in}t) \right| - V_d^*, \quad \text{when SW OFF.} \quad (2)$$

From Fig. 2, the conventional feedforward signal v_{conf} (i.e., the nominal duty ratio pattern) is formulated as

$$v_{conf} = 1 - \frac{\hat{V}_s}{V_d^*} |\sin(2\pi f_{in}t)|. \quad (3)$$

For the assumed significantly high switching frequency f_{tri} , the instantaneous value of $|v_s(t)|$ can be seen as fixed over each switching period. By considering the feedforward loop shown in Fig. 2, the control signal v_{cont} now is the sum of the feedback control signal v_{contb} and the input voltage feedforward signal v_{conf} . Thus, the average duty ratio \bar{d} with conventional feedforward loop now becomes

$$\bar{d} = v_{contb} + 1 - \frac{\hat{V}_s}{V_d^*} |\sin(2\pi f_{in}t)|. \quad (4)$$

By using the time-averaging approach, the two aforementioned equations can be combined to obtain the average inductor voltage through multiplying (1) by turning-ON time $\bar{d}T_s$ and multiplying (2) by turning-OFF time $(1 - \bar{d})T_s$, respectively.

$$v_L = \left| \hat{V}_s \sin(2\pi f_{in}t) \right| - (1 - \bar{d})V_d^*. \quad (5)$$

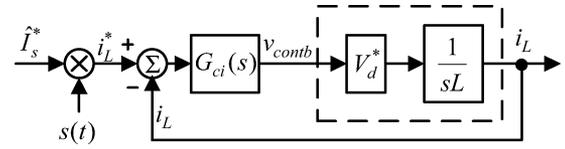


Fig. 3. Equivalent control model with conventional feedforward loop.

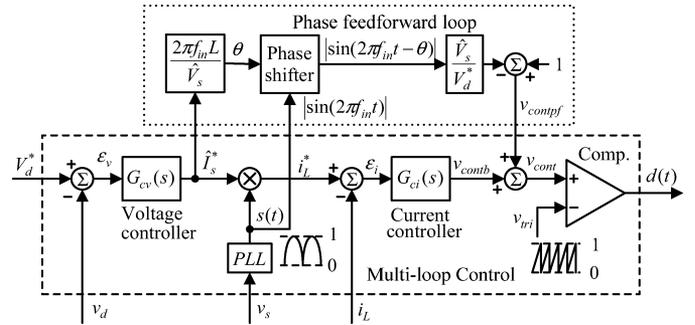


Fig. 4. Multiloop control with proposed phase feedforward loop.

Substituting (4) into (5) enables one to obtain the following simplified equation:

$$v_L = L \frac{di_L}{dt} = v_{contb} V_d^*. \quad (6)$$

Based on (6), the equivalent control model can be plotted in Fig. 3. It shows that the effect of large-scale input voltage variation had been removed from the control loop by introducing the feedforward signal v_{conf} . Obviously, the equivalent plant model in the dashed line of Fig. 3 is a first-order model. It means that the simple proportion-type (P-type) controller can be used in the current controller $G_{ci}(s) = K_p$. Then, the closed-loop transfer function of the inductor current becomes

$$\frac{i_L(s)}{i_L^*(s)} = \frac{K_p V_d^*}{K_p V_d^* + Ls} = \frac{1}{1 + (s/(K_p V_d^*/L))}. \quad (7)$$

III. PROPOSED PHASE FEEDFORWARD CONTROL

Fig. 4 shows the proposed PFFC for boost-type SMRs where its inner current controller is composed of a P-type feedback controller and a phase feedforward loop. Note that the phase feedforward signal v_{conf} is generated from the input current reference magnitude \hat{I}_s^* and the rectified signal $s(t)$.

From Fig. 4, the phase signal θ varies with the input current reference magnitude \hat{I}_s^* and can be expressed as

$$\theta = \frac{2\pi f_{in}L}{\hat{V}_s} \hat{I}_s^*. \quad (8)$$

Then, the PFFC signal v_{conf} now becomes

$$\begin{aligned} v_{conf} &= 1 - \frac{\hat{V}_s}{V_d^*} |\sin(2\pi f_{in}t - \theta)| \\ &= 1 - \frac{\hat{V}_s}{V_d^*} |\sin(2\pi f_{in}t) \cos \theta - \sin \theta \cos(2\pi f_{in}t)|. \end{aligned} \quad (9)$$

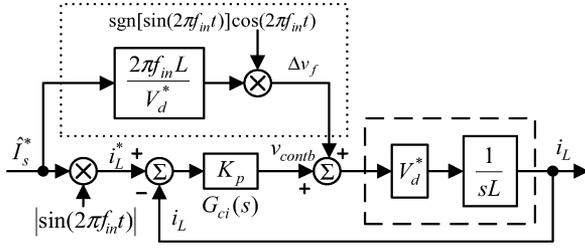


Fig. 5. Equivalent control model with proposed phase feedforward loop.

Assume that the phase θ in radians is near zero ($\theta \approx 0$) and, therefore, $\sin \theta \approx \theta$ and $\cos \theta \approx 1$. By applying the above assumption into (9), the phase feedforward signal v_{contpf} can be approximated as

$$v_{\text{contpf}} \approx 1 - \frac{\hat{V}_s}{V_d^*} |\sin(2\pi f_{in} t)| + \theta \frac{\hat{V}_s}{V_d^*} \text{sgn}(\sin(2\pi f_{in} t)) \cos(2\pi f_{in} t) \quad (10)$$

where $\text{sgn}(\bullet)$ is the sign operator.

By replacing (3) and (8) into (10), we can approximate v_{contpf} in terms of v_{contf}

$$v_{\text{contpf}} \approx v_{\text{contf}} + \hat{I}_s^* \frac{2\pi f_{in} L}{V_d^*} \text{sgn}(\sin(2\pi f_{in} t)) \cos(2\pi f_{in} t) = v_{\text{contf}} + \Delta v_f \quad (11)$$

where Δv_f denotes the difference between the proposed signal v_{contpf} and the conventional signal v_{contf} . The average duty ratio \bar{d} in Fig. 4 can now be expressed by

$$\bar{d} = (v_{\text{contb}} + \Delta v_f) + v_{\text{contf}}. \quad (12)$$

Then, we can substitute (12) into (5) and yield the following equation:

$$L \frac{di_L}{dt} = V_d^* (v_{\text{contb}} + \Delta v_f). \quad (13)$$

Based on (13), the resulting equivalent current control dynamic model is shown in Fig. 5, where the reference current amplitude \hat{I}_s^* is also plotted. Compared to the conventional feedforward loop, the proposed phase feedforward loop introduces an additional term Δv_f into the equivalent control model. As the output power increases, the reference current amplitude \hat{I}_s^* also increases and thus, the proposed term Δv_f increases. It implies that the proposed PFFC can be referred to as a combination of input voltage feedforward control and load feedforward control. Then, from Fig. 5, the closed-loop current tracking transfer function now becomes:

$$\frac{i_L(s)}{i_L^*(s)} = 1. \quad (14)$$

By comparing (14) with (7), we can find that the performance of proposed PFFC has no relation to the current loop parameter.

The proposed PFFC can be seen as a combination of a phase shifter and two “gain” blocks. In analog circuit, it is hard to

TABLE I
SIMULATED CIRCUIT PARAMETERS

Input line voltage (peak)	$\hat{V}_s = 155V$ ($110V_{rms}$)
Triangular signal magnitude	$\hat{V}_{tri} = 1V$
Voltage command	$V_d^* = 250V$
Input line frequency	$f_{in} = 50Hz$
Smoothing capacitance	$C_d = 560\mu F$
Smoothing inductance	$L = 4.65mH$
Equivalent load resistance	$R_L = 100\Omega$
Carrier frequency	$f_{ri} = 25kHz$

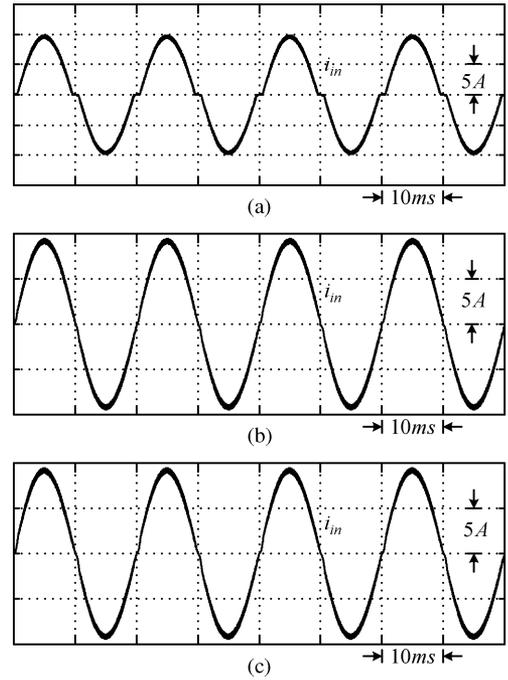


Fig. 6. Input currents for $K_p = 0.597$. (a) Without any feedforward loop. (b) With conventional feedforward loop. (c) With proposed phase feedforward loop.

implement the phase shifter with varying phase. However, it is very easy to implement a phase shifter with varying phase in a digital system (like DSP/FPGA). Therefore, there is near-zero complexity added to the digital implementation of PFFC.

IV. SIMULATION RESULTS

The circuit component values used are listed in Table I and a PI-type controller is used as the voltage controller to regulate the output voltage. Substituting those parameters in Table I into (7) and choosing cutoff frequency $f_c = 5$ kHz and $f_c = 0.5$ kHz obtain the proportion gain of current controller $G_{ci}(s) = K_p = 0.597$ and $K_p = 0.0597$, respectively. For various proportion gain (i.e., various cutoff frequency), the simulated currents without any feedforward loop, with conventional feedforward loop, and with the proposed phase feedforward loop are plotted in Figs. 6 and 7, respectively.

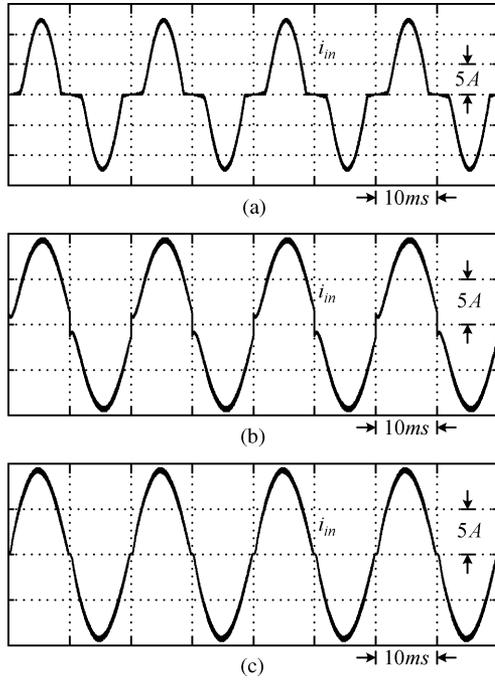


Fig. 7. Input currents for $K_p = 0.0597$. (a) Without any feedforward loop. (b) With conventional feedforward loop. (c) With proposed phase feedforward loop.

Obviously, we can find that the current waveforms are improved through including feedforward loops. When the cutoff frequency f_c ($=5$ kHz) is far larger than the double line frequency $2f_{in}$ ($=100$ Hz), the difference between the responses of conventional feedforward loop and the proposed phase feedforward loop is very small.

When the cutoff frequency f_c ($=500$ Hz) is close to the double line frequency $2f_{in}$ ($=100$ Hz), current responses in Fig. 6(c) are very close to that in Fig. 7(c), which also shows the independence of proportion gain K_p on closed-loop response in (14). In addition, some current drops at zero-crossing points can be found in Fig. 7(b) and such current drops not only lead to the high current harmonics but also result in additional power loss from hard-switching of diode. Consequently, compared to a conventional feedforward signal, relatively small parameter K_p can be used in the proposed PFFC without loss of current tracking performance, which would also increase the overall system immunity against noise.

V. EXPERIMENTAL RESULTS

The proposed PFFC has been digitally implemented in a DSP-based system, where a PI-type voltage controller $G_{cv}(s)$ is used. The experimental circuit components had been listed in Table I. The sampling frequencies of the current loop and voltage loop are 25 kHz and 1 kHz, respectively.

A. Steady-State Performance

In order to illustrate the effectiveness of proposed PFFC, the load resistance $R_L = 80 \Omega$ is chosen to deliver input power near 850 W and the parameter of the current controller is set

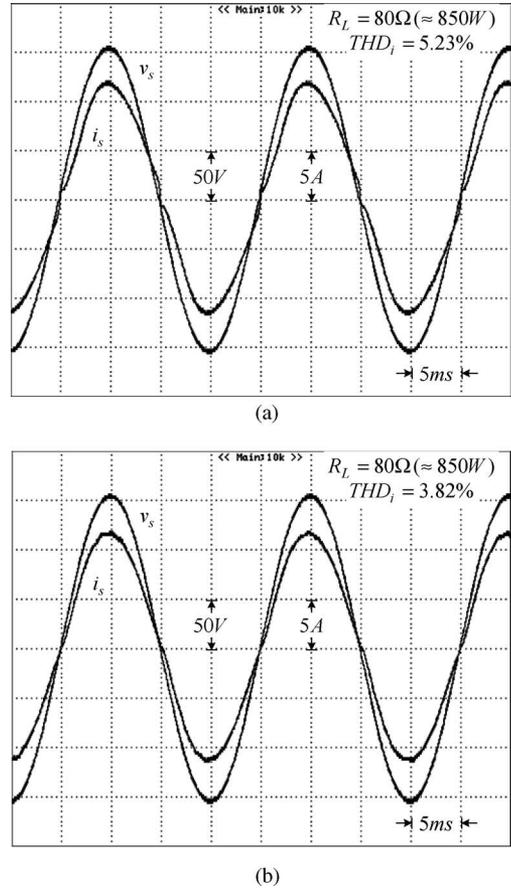


Fig. 8. Experimental input voltage and current for $K_p \approx 0.0597$. (a) With conventional feedforward loop. (b) With proposed phase feedforward loop.

TABLE II
MEASURED TOTAL CURRENT HARMONIC DISTORTION (THD_i) UNDER VARIOUS LOAD RESISTANCES AND VARIOUS FEEDFORWARD LOOPS

R_L	Measured THD_i (%)	
	With Conventional Feedforward Loop	With Proposed Phase Feedforward Loop
	$K_p \approx 0.0597$	$K_p \approx 0.0597$
$80\Omega (\approx 850W)$	5.23	3.82
$100\Omega (\approx 675W)$	5.01	3.97
$133\Omega (\approx 500W)$	4.67	4.37
$200\Omega (\approx 335W)$	5.29	5.33

$K_p \approx 0.0597$. The measured input voltage v_s and input currents i_s with conventional feedforward loop and with proposed phase feedforward loop are plotted in Fig. 8(a) and (b), respectively. By using digital power meter YOGOGAWA WT210, the measured total harmonic current distortion (THD_i) values in Fig. 8(a) and (b) are 5.23% and 3.82%, respectively. It shows that with relatively low proportion gain, the proposed PFFC possesses better feedforward performance than the conventional one. The other measured THD_i values with various load resistances R_L and various feedforward loops are tabulated in Table II.

Like the simulation, negligible difference of THD_i between two feedforward loops can be found by using a relatively high

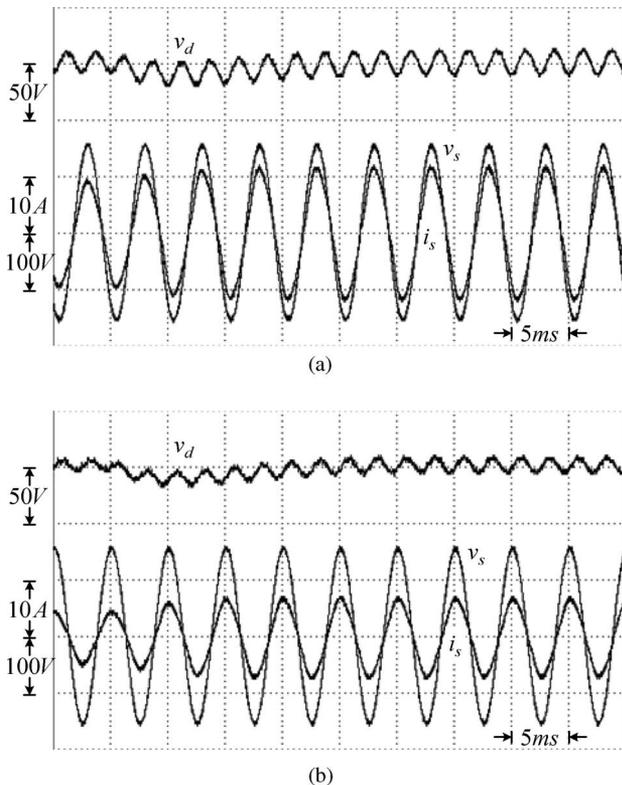


Fig. 9. Measured waveforms during the load resistance change. (a) From $R_L = 100 \Omega$ to $R_L = 80 \Omega$. (b) From $R_L = 200 \Omega$ to $R_L = 133 \Omega$ (Top) Output voltage. (Bottom) Input current and voltage.

proportion gain. But an obvious difference can be found with using smaller proportion gain $K_p \approx 0.0597$, especially at high power (i.e., low load resistance). That is, small proportion gain K_p can be used in the proposed PFFC to increase the system immunity against noise without loss of current dynamic response.

In general, the quantized error of the input signal plays an important role in the experiment especially when the input signal is small. It follows that the quantized error of the inductor current at low load level is larger than it is at relatively high load level, which would result in the dependence of measured THDs on the load level.

In the conventional input voltage feedforward loop, the feedforward signal is fixed regardless of the load level, but the proposed phase feedforward signal adjusts according to the load level. It follows that when the load level is small (i.e., light load), the differences between the two feedforward signals and their performances are small, which can be further confirmed from the close measured THD values at $R_L = 200 \Omega$.

Since the proposed feedforward signal changes according to the load level, we expect to obtain similar THD values at various load conditions. However, due to the decrease of the quantized error with the increase of load level, the measured THD value also decreases.

For the fixed feedforward signal regardless of load level, we expect to obtain increasing THD values with the increase of load level. However, it is noted that the measured THD value initially decreases from $R_L = 200 \Omega$ (335 W) through $R_L = 133 \Omega$ (500 W) and then increases until $R_L = 100 \Omega$ (675 W) due to the decrease of the quantized error with the increase of load level.

B. Transient Performance

To evaluate the transient performance of the proposed PFFC with $K_p \approx 0.0597$, the measured waveforms during the load resistance change from $R_L = 100 \Omega$ to $R_L = 80 \Omega$ and during the change from $R_L = 200 \Omega$ to $R_L = 133 \Omega$ are plotted in Fig. 9(a) and (b), respectively. From Fig. 9, we can find that there is obvious voltage dip in the output voltage v_d due to load change and then, the voltage controller regulates the output voltage to the voltage command $V^* = 250 \text{ V}$ by increasing the current magnitude \hat{I}_s . It shows that the regulation performance of proposed PFFC is also acceptable.

VI. CONCLUSION

In this letter, the phase feedforward loop was proposed for digital implementation of PFC function. Based on the boost-type SMRs, the phase feedforward loop was derived in detail. By using the proposed phase feedforward loop, we can use a simple P-type current controller with relatively small gain and yield variable feedforward signals according to the load condition. Simulated and experimental results further demonstrate and confirm the benefits of the proposed PFFC, particularly for those applications whose current closed-loop cutoff frequency is close to the double line frequency.

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